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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Markus SCHETELIG, et al.

Application No.: Not yet Assigned

Filing Date: December 21, 2001

Title: SIGNAL DC OFFSET CORRECTION METHOD AND DEVICE

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

December 21, 2001

Sir:

Prior to examination, please amend the above-identified application as follows.

IN THE CLAIMS:

Please amend claims 1-15 to read as follows:

1. A method for correcting the direct current offset portion (DC offset) of a first signal comprising the steps of:

- phase shifting said first signal for obtaining a second signal
- comparing said first signal and said second signal with an estimated DC offset.

2. A method according to claim 1 characterised in that said estimated DC offset is adjusted if the result of the comparison is, that said first signal and said second signal are on different sides of said estimated DC offset.

3. A method according to claim 1 characterized in that said estimated DC offset is kept constant if the result of the comparison is, that said first signal and said second signal are on the same side of said estimated DC offset.

4. A method according to claim 1 characterised in that said phase shifted second signal is obtained by low pass filtering said first signal.

5. A method according to claim 1 characterised in that it is used for correcting the DC offset portion of a received and demodulated radio frequency signal.

6. A method according to claim 5 characterised in that said demodulation is a demodulation for GFSK modulated signals.

7. A device for adjusting the direct current offset portion (DC offset) of a signal comprising:

- an input for connecting to a signal line for receiving said signal
- a phase shifting element connected to the input for producing a phase shiftedsignal
- means for adjusting said estimated DC offset if said phase shifted signal is connected to its input and holding said estimated DC offset if said phase shifted signal is disconnected from its input.
- an output signal line connected to the output of said said means for adjusting said estimated DC offset
- a decision circuit for deciding if said signal and said phase shifted signal on different or same sides of said estimated DC offset,
- a switch for connecting said phase shifted signal to said means for adjusting said estimated DC offset if said decision circuit decides that said signal and said phase shifted

siganl are on different sides of said estimated DC offset and disconnecting said phase shifted input signal from said means for adjusting said estimated DC offset if the decision circuit decides that said signal and said phase shifted signal are on the same side of said estimated DC offset .

8. A device according to claim 7 characterised in that said means for phase shifting said signal is a low pass filter.

9. A device according to claim 7 characteristed in that said means for adjusting said estimated DC-offset is a low pass filter.

10. A device according to claim 7 characterised in that said decision circuit comprises:

a first and a second comparator circuit with input signal lines X and input signal lines Y comparing input signals X and Y, whereby the input signal line X of the first comparator circuit is connected to the output of said means for phase shifting said signal and the input signal line X of the second comparator circuit is connected to the input signal and the input signal lines Y of the first and second comparator circuits are connected to the output signal line; an Exclusive-OR gate comprising two input signal lines and the output of said XOR gate controlling the switch, whereby the outputs of the first and second comparator circuit are connected to the input lines of said XOR gate.

11. A radio frequency receiver comprising a device for correcting the DC offset according to claim 7 implemented as an analog circuit as part of said receiver.

12. An electronic device comprising a device for correcting the DC offset according to claim 7 implemented as a digital hardwired logic.

13. A device according to claim 7 for correcting the DC offset of a received and demodulated radio frequency signal.

14. A transceiver comprising a device for correcting the DC offset according to claim 7.

15. A communication device comprising a device for correcting the DC offset according to claim 7.

In the Abstract

Please amend the Abstract to read as follows:

The invention relates to a method and a device for estimating the DC offset portion of a signal, especially of a signal containing parts with sinusoidal shaping, for example a signal which results from demodulation of a frequency modulated receive signal.

According to the invention a method is presented for correcting the direct current offset portion of a first signal which comprises the following steps: - phase shifting the first signal for obtaining a second signal; comparing the first signal and the second signal with an estimated DC offset. The estimated DC offset is adjusted if the result of the comparison is, that the first signal and the second signal are on different sides of said estimated DC offset and the estimated DC offset is kept constant as long as the result of the comparison is, that the first signal and the second signal are on the same side of the estimated DC offset.

REMARKS

Attached hereto is a marked-up version of the changes made to the claims and Abstract by the current preliminary amendment. The attached page is captioned **"Version with markings to show changes made."**

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, or credit any overpayment of fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.35359X00).

Respectfully submitted,

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Attachment

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims

1. A method for correcting the direct current offset portion ~~(DC offset)~~ of a first signal ~~(Signal 1)~~ comprising the steps of:

- phase shifting said first signal ~~(Signal 1)~~ for obtaining a second signal ~~(Signal 2)~~
- comparing said first signal ~~(Signal 1)~~ and said second signal ~~(Signal 2)~~ with an estimated DC offset.
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2. A method according to claim 1 characterised in that said estimated DC offset is adjusted if the result of the comparison is, that said first signal ~~(Signal 1)~~ and said second signal ~~(Signal 2)~~ are on different sides of said estimated DC offset.

3. A method according to claim 1 characterized in that said estimated DC offset is kept constant if the result of the comparison is, that said first signal ~~(Signal 1)~~ and said second signal ~~(Signal 2)~~ are on the same side of said estimated DC offset.

4. A method according to ~~any of~~ claim~~s~~ 1 ~~to 3~~ characterised in that said phase shifted second signal ~~(Signal 2)~~ is obtained by low pass filtering said first signal ~~(Signal 1)~~.

5. A method according to ~~any of~~ claim~~s~~ 1 ~~to 4~~ characterised in that it is used for correcting the DC offset portion of a received and demodulated radio frequency signal.

6. A method according to ~~any of~~ claim~~s~~ ~~1 to~~ 5 characterised in that said demodulation is a

demodulation for GFSK modulated signals.

7. A device for adjusting the direct current offset portion (DC offset) of a signal ~~(Signal 1)~~ comprising:

- an input for connecting to a signal line for receiving said signal ~~(Signal 1)~~
- a phase shifting element ~~(LPF 1)~~ connected to the input for producing a phase shiftedsignal ~~(Signal 2)~~
- means ~~(LPF2)~~ for adjusting said estimated DC offset if ~~Signal 2~~ said phase shifted signal is connected to its input and holding said estimated DC offset if ~~Signal 2~~ said phase shifted signal is disconnected from its input.
- an output signal line ~~(OUT)~~ connected to the output of said said means for adjusting said estimated DC offset ~~(LPF 2)~~
- a decision circuit ~~(DEC)~~ for deciding if ~~Signal 1~~ said signal and ~~Signal 2~~ said phase shifted signal are on different or same sides of said estimated DC offset,
- a switch ~~(SW)~~ for connecting said phase shifted signal ~~(Signal 2)~~ to said means for adjusting said estimated DC offset ~~(LPF2)~~ if said decision circuit decides that ~~Signal 1~~ said signal and ~~Signal 2~~ said phase shifted signal are on different sides of said estimated DC offset ~~(switch position A)~~ and disconnecting said phase shifted input signal ~~(Signal 2)~~ from said means for adjusting said estimated DC offset ~~(LPF2)~~ if the decision circuit decides that ~~Signal 1~~ said signal and ~~Signal 2~~ said phase shifted signal are on the same side of said estimated DC offset ~~(switch position B)~~.

8. A device according to claim 7 characterised in that said means for phase shifting said signal ~~(Signal 1)~~ is a low pass filter ~~(LPF 1)~~.

9. A device according to claim 7 ~~or 8~~ characteristed in that said means for adjusting said

estimated DC-offset is a low pass filter ~~(LPF 2)~~.

10. A device according to ~~one of~~ claims 7 ~~to 9~~ characterised in that said decision circuit ~~(DEC)~~ comprises:

- a first and a second comparator circuit ~~(DEC 1.1; DEC 1.2)~~ with input signal lines X and input signal lines Y comparing input signals X and Y, whereby the input signal line X of the first comparator circuit ~~(DEC 1.1)~~ is connected to the output of said means for phase shifting ~~signal 1~~ said signal and the input signal line X of the second comparator circuit ~~(DEC 1.2)~~ is connected to the input signal ~~(Signal 1)~~ and the input signal lines Y of the first and second comparator circuits are connected to the output signal line ~~(OUT)~~; an Exclusive-OR ~~(XOR)~~ gate comprising two input signal lines and the output of said XOR gate controlling the switch ~~(SW)~~, whereby the outputs of the first and second comparator circuit ~~(DEC 1.1; DEC 1.2)~~ are connected to the input lines of said XOR gate.

11. A radio frequency receiver comprising a device for correcting the DC offset according to ~~one of~~ claims 7 ~~to 10~~ implemented as an analog circuit as part of said receiver.

12. An electronic device comprising a device for correcting the DC offset according to ~~one of~~ claims 7 ~~to 10~~ implemented as a digital hardwired logic.

13. A device according to ~~one of~~ claims 7 ~~to 12~~ for correcting the DC offset of a received and demodulated radio frequency signal.

14. A transceiver comprising a device for correcting the DC offset according to ~~one of~~ claims 7 ~~to 13~~.

15. A communication device comprising a device for correcting the DC offset according to ~~one of~~ claims 7 ~~to 13~~.

In the Abstract

The invention relates to a method and a device for estimating the DC offset portion of a signal, especially of a signal containing parts with sinusoidal shaping, for example a signal which results from demodulation of a frequency modulated receive signal.

According to the invention a method is presented for correcting the direct current offset portion ~~(DC offset)~~ of a first signal ~~(Signal 1)~~ which comprises the following steps: - phase shifting the first signal ~~(Signal 1)~~ for obtaining a second signal ~~(Signal 2)~~; comparing the first signal ~~(Signal 1)~~ and the second signal ~~(Signal 2)~~ with an estimated DC offset. The estimated DC offset is adjusted if the result of the comparison is, that the first signal ~~(Signal 1)~~ and the second signal ~~(Signal 2)~~ are on different sides of said estimated DC offset and the estimated DC offset is kept constant as long as the result of the comparison is, that the first signal ~~(Signal 1)~~ and the second signal ~~(Signal 2)~~ are on the same side of the estimated DC offset.